

Tristan Lee

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SUMMARY

Electrical Engineering student specializing in Signal and Image Processing, with a minor in Cognitive Science (Neuroscience). Most of my work is embedded firmware and signal processing for neurotech, from EMG prosthetic control at Triton NeuroTech to gaze-tracking research at the Veale Lab, Kyoto University. I also design FPGA market-data hardware with Triton Quantitative Trading.

EDUCATION

University of California, San Diego

September 2025 - June 2028

B.S. in Electrical Engineering (Signal & Image Processing), Minor in Cognitive Science

La Jolla, California

- **Relevant Coursework:** OOP in C++, Engineering Computation in C, Digital Design, Analog Design, Circuits & Systems, Probability & Statistics, Data Science in Practice
- **Activities:** Triton NeuroTech, Triton Quantitative Trading, Triton Solar Car, IEEE, UCSD Ice Hockey, UCSD Surf Club

Kyoto University

April 2026 - August 2026

International Exchange - Research Student (KUINEP)

Kyoto, Japan

- **Relevant Coursework:** Behavioral Neuroscience, Fundamentals of Artificial Intelligence, Basics of AI and Informatics
- **Activities:** Developmental Neurorobotics Lab (Veale Lab), KU Ice Hockey Team

Evergreen Valley College

August 2023 - January 2026

A.S. in Mathematics, Computer Science, & Physics

San Jose, California

- **Relevant Coursework:** Foundations of Data Science, Data Structures, Programming & Methodology
- **Activities:** President - EVC Engineering Club, Vice President - EVC Computer Science Club

CERTIFICATIONS

Anthropic: AI Fluency: Framework & Foundations, AI Fluency for Students, Claude 101, Claude Code in Action, Introduction to Model Context Protocol, Introduction to Agent Skills | **NASA:** Community College Aerospace Scholar

SKILLS

Programming: Python, C/C++, SystemVerilog, Verilog, Swift, Java, JavaScript, MATLAB, HTML/CSS, LaTeX

Data & Visualization: Pandas, NumPy, Matplotlib, Jupyter, statistical analysis, data cleaning

Tools & Hardware: Vivado, Xilinx Alveo U55C, Arduino, ESP32, EMG sensors, Tobii Pro Glasses 3, Onshape, KiCad

EXPERIENCE

Triton NeuroTech

October 2025 - Present

Project Lead, sEMG Soft Exosuit (2026-27); Firmware Engineer, Software Sub-team (2025-26)

La Jolla, California

- Leading the 2026-27 BCI-track team building an sEMG-controlled soft exosuit for hand and wrist rehabilitation.
- Programmed Arduino microcontrollers in C++ to read EMG data and drive motors for prosthetic hand control.
- Configured pins and tuned signal thresholds for responsive sensor-to-actuator control, then documented board setups and baseline firmware for the mechanical team.

Developmental Neurorobotics Lab (Veale Lab), Kyoto University

April 2026 - Present

Research Assistant, Graduate School of Medicine

Kyoto, Japan

- Optimized a Tobii Pro Glasses 3 gaze-overlay pipeline in Python, replacing per-frame pandas filtering with vectorized NumPy timestamp lookups.
- Ran exploratory data analysis on a control baseline gaze dataset and presented the findings to the lab.
- Built a native macOS head-tracking prototype in Swift (AVFoundation, Vision) for a lab demonstration.

Triton Quantitative Trading

February 2026 - Present

FPGA / RTL Design Engineer

La Jolla, California

- Developing an ITCH 5.0 decoder in SystemVerilog that parses NASDAQ feeds off a 100G CMAC interface and updates Limit Order Book registers for live top-of-book output.

NASA - California Space Grant Consortium Microcomputer & Robotics

May 2025 - August 2025

Engineering Intern

San Jose, California

- Engineered embedded C++ firmware for an ESP32-based algae detection robot, integrating turbidity, pH, and temperature sensors to log over 1,000 readings for environmental monitoring.
- Wrote Python workflows that automated calibration, processed sensor data in real time, and plotted results to speed up testing.
- Documented the calibration and firmware deployment process. Received the CSGC Award of Excellence.

TECHNICAL PROJECTS

ITCH 5.0 Parser & Limit Order Book

- Designed an FPGA-based NASDAQ market data decoder and Limit Order Book in pure Verilog, achieving sub-840ns end-to-end latency on a Xilinx Alveo U55C as part of a 6-person HFT pipeline.
- Implemented a 512-bit AXI-Stream adapter and byte-serial finite state machine to parse all four ITCH 5.0 message types, validated in Vivado simulation against real NASDAQ data with 0 errors and synthesized at 100MHz with 8.71ns timing slack.